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REMARKS

Final Office Action Premature.

Claims 1-20 are pending in the application. The Office Action has been designated as final.[1]

Applicants believe this designation has been made in error.

A final rejection is proper on a second action, except where the examiner introduces a new ground of rejection not necessitated by amendment of the application by the applicant.[2] In the present case, Applicant has submitted only one response to an office action, and this response made no amendments to claims.[3]

In the first Office Action issued for this case, dated 10/12/2005, various claims were rejected based on U.S. Patent Publication No. 2001/0046163 (referred to hereafter as *Yanagawa*):

> Claims 1, 5, 7-19 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Yanagawa (US Patent Application Publication 2001/0046163). (Office Action, dated 10/12/2005, Page 3, Lines 1-2).

Importantly, claims 2 and 20 were not rejected based on this reference.

However, in the present Final Office Action, an entirely new ground for rejection has been presented, as claim 2 is newly rejected, based on *Yanagawa*:

> Claims 1-*2*, 5, 7-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Yanagawa (US Patent Application Publication 2001/0046163). (Final Office Action, dated 02/06/2006, Page 6, Lines 1-

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[1] See the Office Action, dated 02/06/06, Page 1 (Office Action Summary), Section "Status".

[2] MPEP § 706.07(a).

[3] See Applicant's Response Office Action, dated 01/09/06, Page 3.

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2).

Thus, the present Final Office Action presents a new ground of rejection for both claims 2 and 20, denying Applicant a fair opportunity to address and/or amend the claims in light of the rejection.

For these reasons, it is respectfully requested that the finality of the last Office Action be reconsidered, and Applicant be presented with the opportunity to address the new grounds of rejection or establish right of petition on this matter.

Respectfully Submitted,

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D. Remarks

Rejection of Claims 1, 5, 7-19 and 21 Under 35 U.S.C. §102(e) based on *Yanagawa* (US Patent Application Publication 2001/0046163 A1).

The rejection of claims 1-2, 5, and 7-14 will first be addressed.

The invention of claim 1 is directed to a memory controller connected to a semiconductor memory device. The memory controller includes a clock generating circuit, a data generating circuit, "m" data output terminals, and m output holding circuits. The output holding circuits are for storing the output digital data synchronously with the output clock signal. Also included are "n" signal output terminals that provide output strobe signals to the semiconductor memory device in synchronism with the output data, where n < m. A plurality of output delay circuits are included, one output delay circuit for every "p" signal output terminal(s). Each output delay circuit delays the output clock signal by a predetermined amount to transmit an output strobe signal to the corresponding p signal output terminal(s). Each output holding circuit is physically adjacent to a corresponding one of the m data output terminals. Further, the output of each output delay circuit is adjacent to the corresponding p signal output terminal(s)

As is well established, a prima facie showing of anticipation requires the presence of a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention.[1]

Applicant's amended claim 1 recites a number of features that believed to be neither shown in nor suggested by the cited reference *Yanagawa*.

Yanagawa is not believed to show or suggest a plurality of output delay circuits, as recited in claim 1. According to Applicant's claim 1, each output delay circuit

1) delays the ***output*** clock signal

2) transmits an ***output strobe*** signal to the corresponding signal output terminal(s), where the signal output terminal provides output strobe signals to the semiconductor memory device in synchronism with the output data.

To show Applicant's plurality of output delay circuits, the rejection points to various

[1] Scripps Clinic & Research Found. v. Genetech Inc., 18 USPQ 2d 1001, 1010 (Fed. Cir. 1991).

figures of *Yanagawa*:

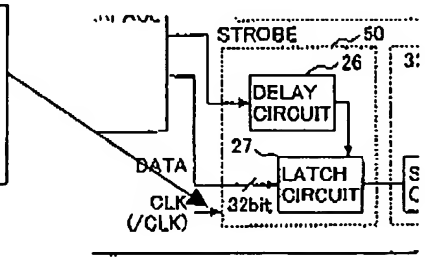
> As to claim 1, Yanagawa discloses... a plurality of delay circuits... [figure 3 shows a plurality of delay circuits; figures 8-11; figure 15; figure 25...] (see the Final Office Action, dated 02/06/2006, Page 6, last line to Page 7, line 2).

These figures cannot show Applicant's output delay circuits, as these circuits are all directed to input delay circuits. This clear difference will be discussed in detail with reference to FIG. 3 of *Yanagawa*. FIG. 3 of *Yanagawa* shows a data acquisition circuit of FIG. 1:

> FIG. 3 is a block diagram of a first embodiment of the data acquisition circuit 50 according to the present invention. [*Yanagawa*, paragraph [0055]].

However, this data acquisition circuit that does essentially the opposite of Applicant's claim language. The data acquisition circuit delays and ***input*** clock signal CLK, not an output clock signal:

Data acquisition circuit 50 delays an input clock signal, not an output clock signal, as indicated by the arrow showing the signal is an input signal.



Thus, the reference does not show an arrangement in which "each output delay circuit delays the output clock signal by a predetermined amount" as recited in claim 1.

Further, the data acquisition circuit of FIG. 3 does not include output delay circuits that each "transmit an ***output strobe*** signal to the corresponding signal output terminal(s)". That is, claim 1 recites multiple output delay circuits that transmit multiple output strobe signals to multiple signal outputs. FIG. 3 shows an arrangement in which one delay circuit that transmits one input strobe signal away from a strobe input:

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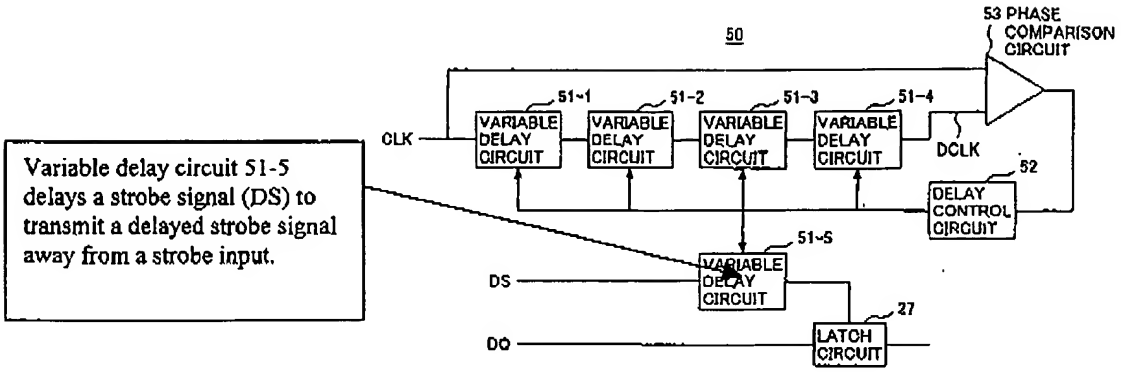

Applicant notes that the remaining figures of *Yanagawa* relied upon to show Applicant's output delay circuits show the same sort of arrangement.

Accordingly, the reference cannot show Applicant's plurality of output delay circuits, as recited in claim 1.

Applicant's claim 2 includes still further limitations not shown in, or suggested by the cited reference. These limitations include:

1) output holding circuits linearly aligned with one another;

2) signal output terminals linearly aligned with output data terminals;

3) output delay circuits linearly aligned with one another between the holding circuits and the aligned data output terminals/signal output terminals.

Yanagawa discloses a memory controller with a data latch operation. However, the reference is entirely silent as to the alignment of any circuit features, let alone the very particular features recited in claim 2.

To show the above emphasized claim limitations, the rejection points to FIG. 2 of *Yanagawa*, and argues certain features are "consistent" with certain of Applicant's figures:

> As to claim 2, Yanagawa teaches that the m output data terminals and n signal output terminals are linearly aligned with one another [figure 2 shows that the 32-bit DATA terminals are physically located at the left-had side of the INTERFACE unit, and there is one-to-one correspondence between the two groups of 32-bit DATA signals... (Final Office Action, dated 02/06/2006, Page 7, Lines 8-13).

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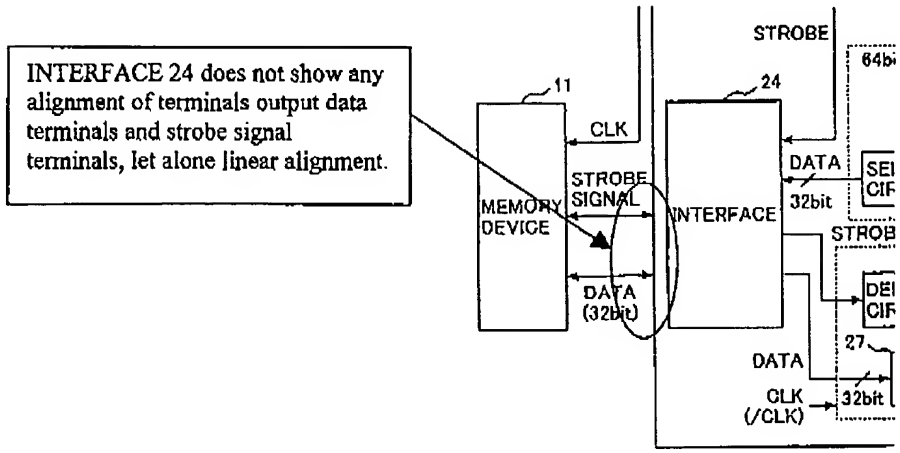
Applicant notes that FIG. 2 of *Yanagawa* shows 32-bit data. However, this figure shows no alignment of any of the above emphasized claim features:



Applicant notes that the text provides no inherent teaching of such a feature, either. A review of the discussion of FIG. 2 in *Yanagawa* (see paragraphs [0048] to [0054] of the reference) provides no mention of any terminals, or alignment of any features.

For all of these reasons this ground for rejection is traversed.

Claim 8 is believed to be separately patentable over the cited reference.

Claim 8, which depends from claim 1, recites a plurality of data input terminals that receive input data from the semiconductor memory device, a signal input terminal for every "q" data input terminals, an input delay circuit corresponding to each signal input terminal, and an input holding circuit corresponding to each data input terminal. Claim 8 further recites, a first wiring corresponding to each data input terminal that transmits digital data to a corresponding input holding circuit, and a second wiring corresponding to each input holding circuit that transmits the input strobe signal from a corresponding input delay circuit to the input holding circuit. The first and second wiring corresponding to each input holding circuit are essentially equal in length.

The above emphasized limitations directed to first and second wiring lengths are not believed to be shown or suggested by the cited reference.

Yanagawa provides no teachings related to wiring, let alone wiring lengths. A word search of *Yanagawa* with the term wir$ (where $ is a wildcard) provides no matches. To show

Applicant's claim 8 limitations, the rejection points to the following teachings in the cited reference:

> Even when the delay of the variable delay circuits varies due to a variety of variation factors such as variation of the manufacturing process, variation in ambient temperature, and variation in the power supply voltage, proper delay control based on the phase comparison of clock signals makes it possible to adjust the delay of the variable delay circuit 51-5 to be equal to the 1/4 cycle of the clock signal. Under the conditions in which a variety of variation factors are present, therefore, optimum data acquisition timing can be achieved. (*Yanagawa*, paragraph [0064]).

The above teaching is clearly not explicitly related to wiring lengths. Further, the above is directed to delaying a clock signal, and not related to any data signals. Applicant's claim 8 recites "a first wiring corresponding to each data input terminal that transmits digital data". The above is unrelated to any line for transmitting data.

Accordingly, because the reference *Yanagawa* does not mention any wiring, and provides no teachings related to wiring lengths and/or delays of digital data, the reference is not believed to show or suggest "a first wiring" and "second wiring" as recited in claim 8.

Claim 14 is also believed to be separately patentable.

Claim 14, which depends from claim 1 via claim 13, recites that data output terminals are data input/output (I/O) terminals, the signal output terminals are signal I/O terminals, and m input holding circuits corresponding to the data I/O terminals formed in the interface region. Each input holding circuit comprises a second latch circuit connected to a corresponding data I/O terminal by a first wiring. An input delay circuit connected to each signal I/O terminal by a second wiring. Each input delay circuit delays a received device input clock from the semiconductor memory device signal by a predetermined amount to generate an input strobe signal. Each input strobe signal being connected to a corresponding second latch circuit by a third wiring. The length of the first wiring to each second latch circuit is essentially equal to the sum of the lengths of the second and third wirings corresponding to the same second latch circuit.

To address this ground for rejection Applicant incorporates by reference herein the same general comments set forth above for claim 8. Namely, that the reference provides no teachings

related to wiring in general, and no teachings related to delaying or wiring of data signals in particular.

The rejection of claims 15-21 will now be addressed.

The memory controller of claim 15 includes a predetermined number "m" data input terminals, a predetermined "n" signal input terminals, a data storing circuit, n input delay circuits, m input holding circuits, m signal input wirings and m signal input wirings. The predetermined number "m" data input terminals receive input data from the semiconductor memory device. Each signal input terminal receiving a device input clock signal from the semiconductor memory device in synchronism with the input data, where m > n. The data storing circuit receives digital data from the data input terminals. The n input delay circuits delay received device input clock signals from the semiconductor memory device by a predetermined amount to generate input strobe signals. The m input holding circuits hold the input data in synchronism with the input strobe signals generated by the input delay circuits. Each data input wiring transmits an input data value from one data input terminal to a corresponding input holding circuit. The m signal input wirings transmit one input strobe signal from one input delay circuit to a corresponding input holding circuit. The data input wiring and signal input wiring for the same corresponding input holding circuit being essentially equal in length.

To address this ground for rejection, Applicant incorporates by reference herein the comments set forth above for claims 8 and 14 are incorporated by reference herein. Namely, because the reference never mentions wiring, it cannot show particular wiring lengths as recited in claim 15.

Claim 20 is believed to be separately patentable over the cited reference.

Claim 20, which depends from claim 15, recites that m data input terminals and n signal input terminals are linearly aligned with one another. In addition, m input holding circuits are linearly aligned with one another parallel to the data input terminals and signal input terminals.

To address this ground for rejection, Applicant incorporates by reference the comments directed to the "linearly aligned" limitations of amended claim 1.

Rejection of Claims 3, 4, and 6 Under 35 U.S.C. §103(a), based on *Yanagawa* in view of *Kuge* (US Patent Application Publication 2001/0014922 A1).

As is well known, in proceedings before the Patent and Trademark Office, the examiner bears the burden of establishing a prima facie case of obviousness based on the prior art.[2]

To establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.[3]

To the extent that this ground for rejection relies on *Yanagawa*, the arguments set forth above with respect to amended claim 1 are incorporated herein by reference. Namely, *Yanagawa* does not show or suggest various limitations of the claim. *Kuge* also does not teach such a limitation element.

For this reason this ground for rejection is traversed.

[2] Ex parte Obukowicz, 27 USPQ 1063, 105 (B.P.A.I. 1992).
[3] MPEP §2143.

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Claim 7 has been amended. Claim 7 has been amended, not in response to the cited art, but to address a typographical error.

The present claims 1-21 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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